

Sheet: Power



File: power.sch

Sheet: FPGA Core Power



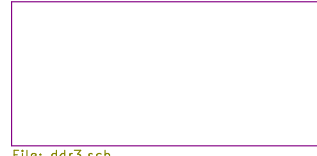
File: fpga_pwr.sch

Sheet: Debug Interface



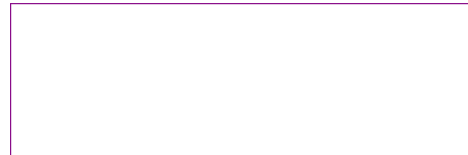
File: debug.sch

Sheet: DDR3



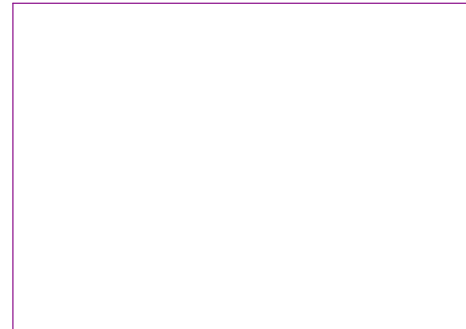
File: ddr3.sch

Sheet: PCIe + SATA



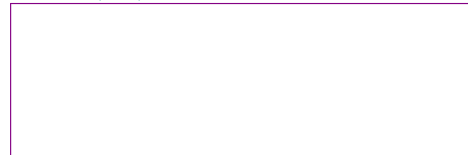
File: serdes.sch

Sheet: FPGA IO



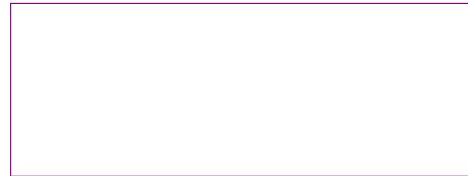
File: fpga_io.sch

Sheet: HDMI, GbE, USB



File: ports.sch

Sheet: Misc IO



File: miscio.sch

1 J16
 MOUNT
 1 MountingHole:MountingHole_3.2mm_M3_Pad
 MOUNT
 MountingHole:MountingHole_3.2mm_M3_Pad

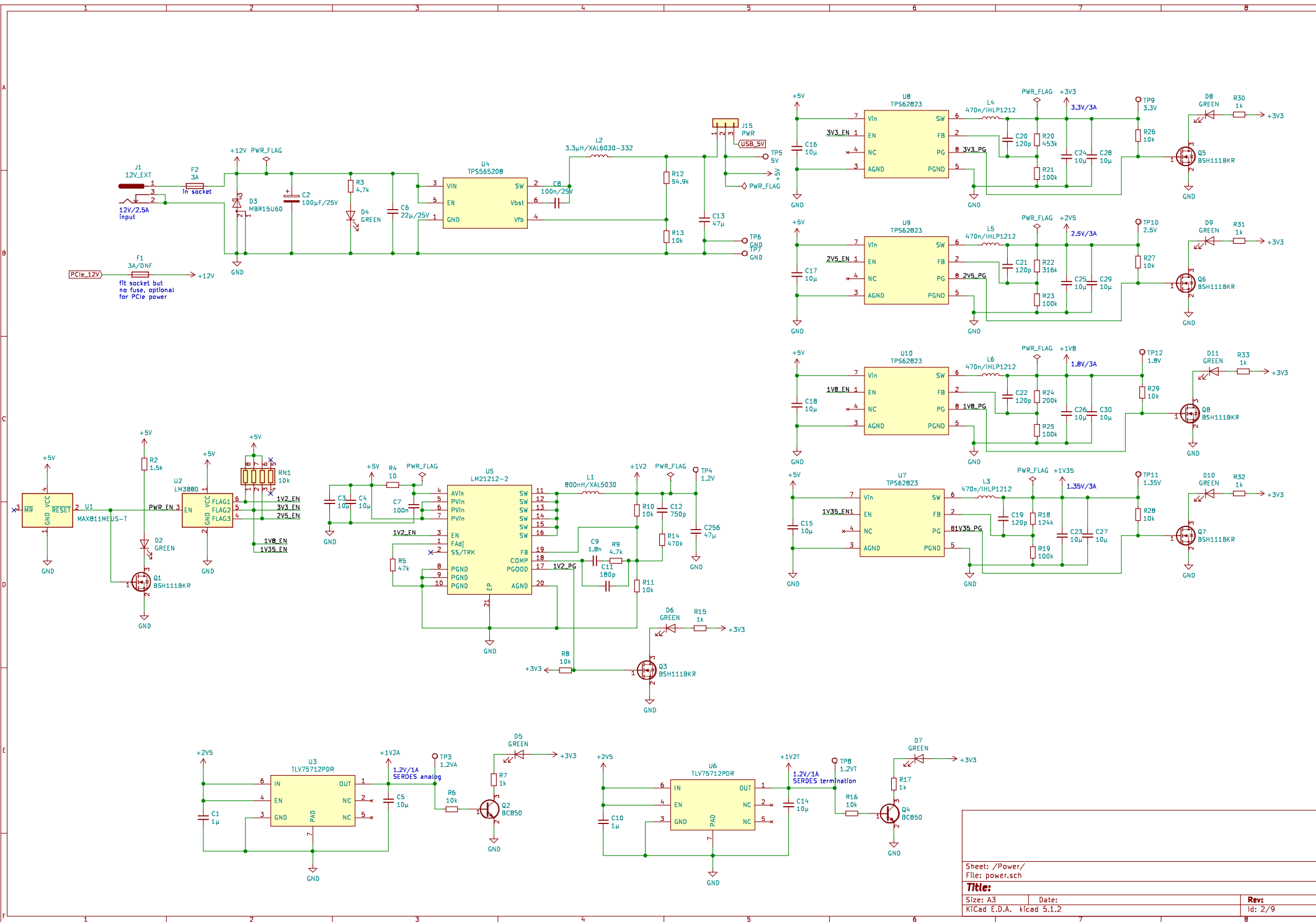
David Shah

Sheet: /
File: ecp5_mainboard.sch

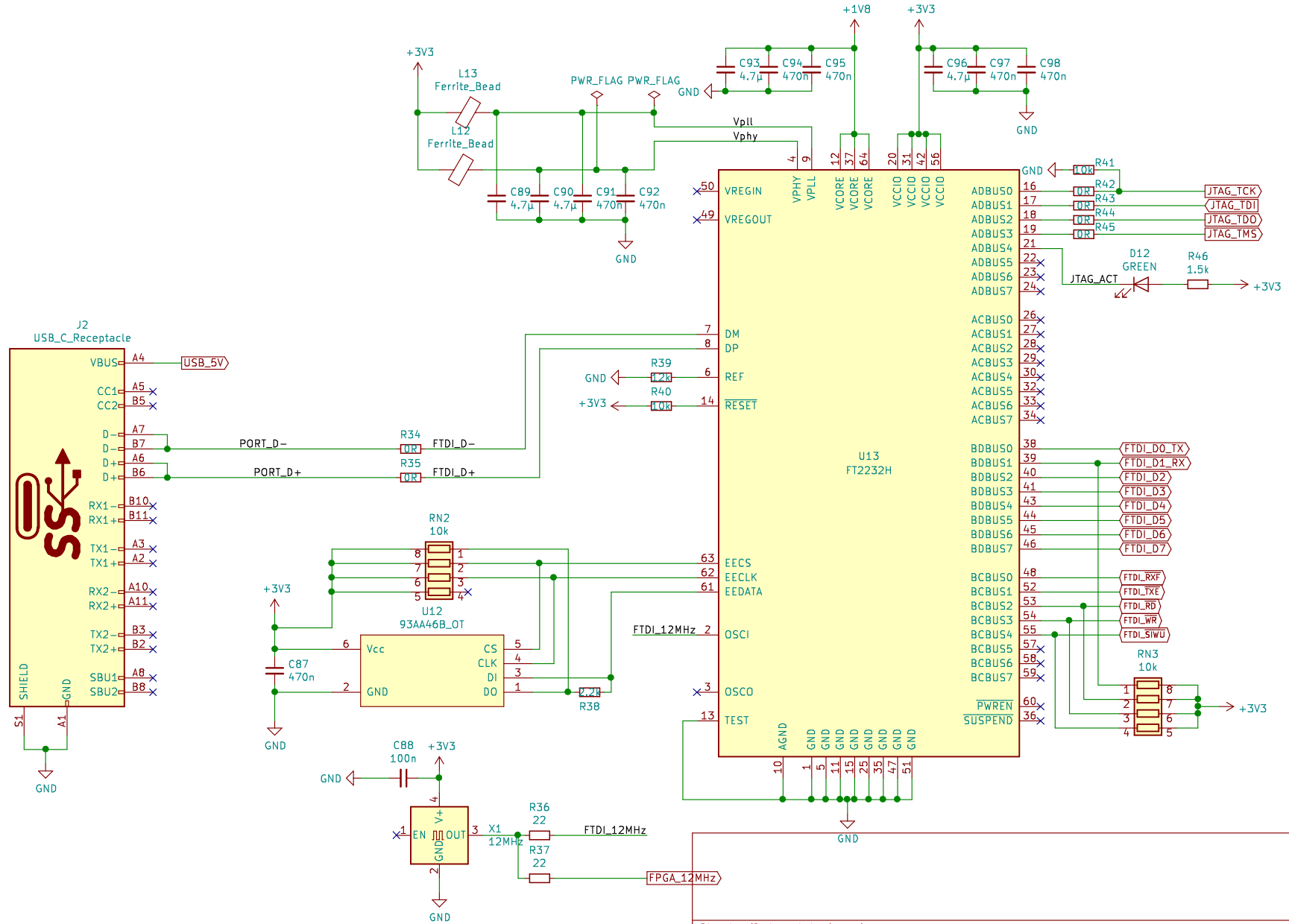
Title: TrellisBoard

Size: A4	Date: 2018-11-20
KiCad E.D.A. kicad 5.1.2	

Rev: 1.0
Id: 1/9



Sheet: /Power/ File: power.sch		
Title:		
Size: A3	Date:	Rev:
KiCad E.D.A. kicad 5.1.2		id: 2/9

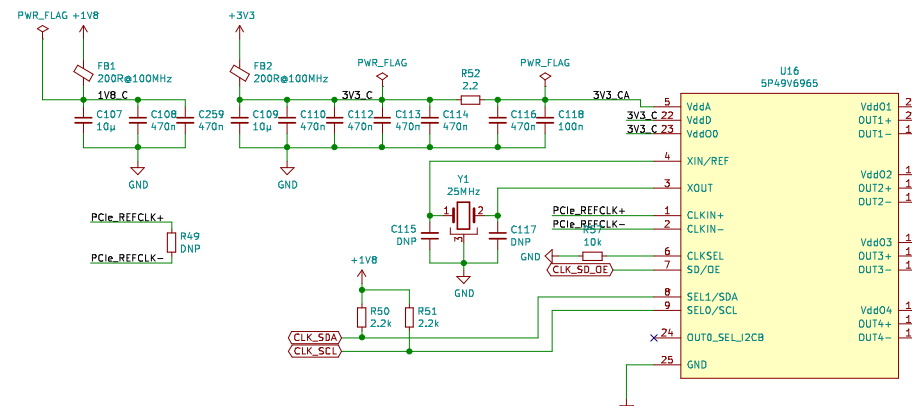
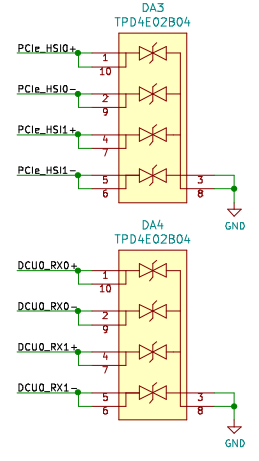
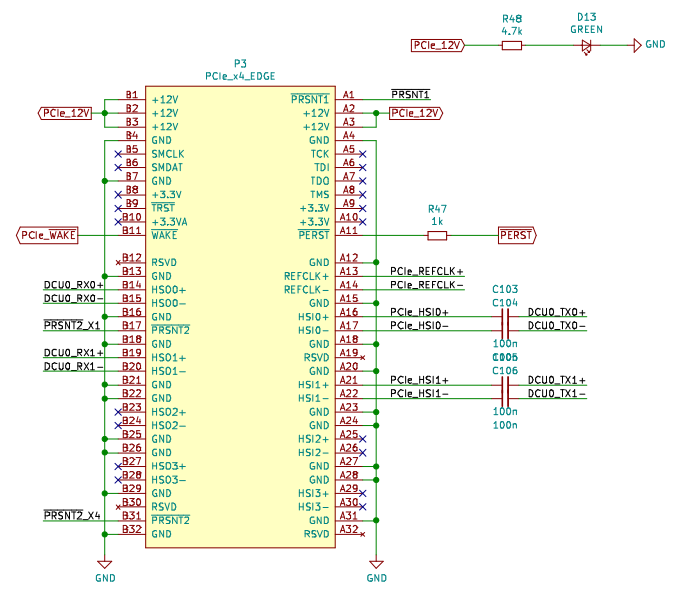


Sheet: /Debug Interface/
File: debug.sch

Title:

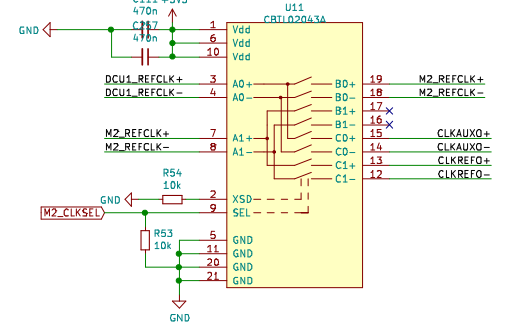
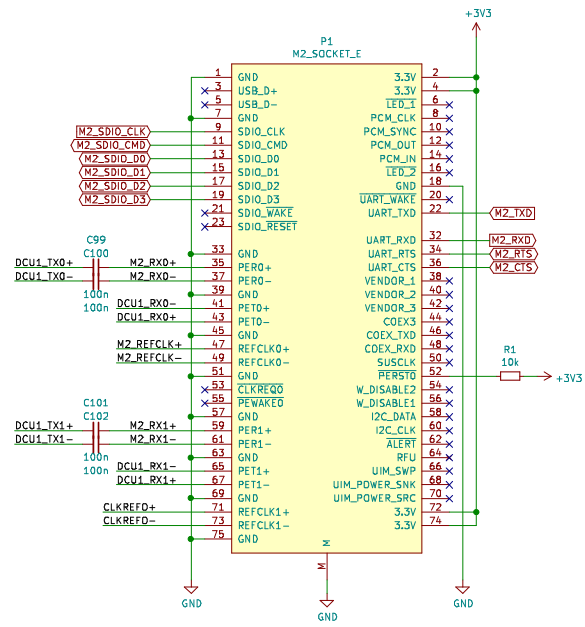
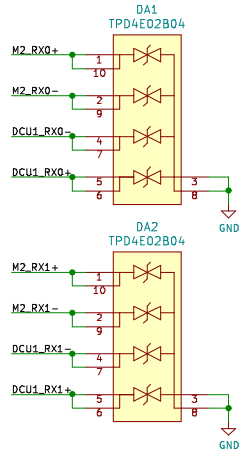
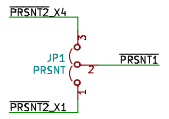
Size: A4 Date:
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Rev:
Id: 4/9



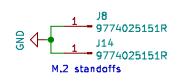
DCU0_TX0+	AK9	HDTXP0_D0CH0
DCU0_TX0-	AK10	HDTXN0_D0CH0
DCU0_RX0+	AM8	HDRXP0_D0CH0
DCU0_RX0-	AM9	HDRXN0_D0CH0
DCU0_TX1+	AM11	HDRXP0_D0CH1
DCU0_TX1-	AM12	HDTXN0_D0CH1
DCU0_RX1+	AK13	HDRXP0_D0CH1
DCU0_RX1-	AK14	HDTXN0_D0CH1
DCU0_REFCLK+	AM14	REFCLKP_D0
DCU0_REFCLK-	AM15	REFCLKN_D0

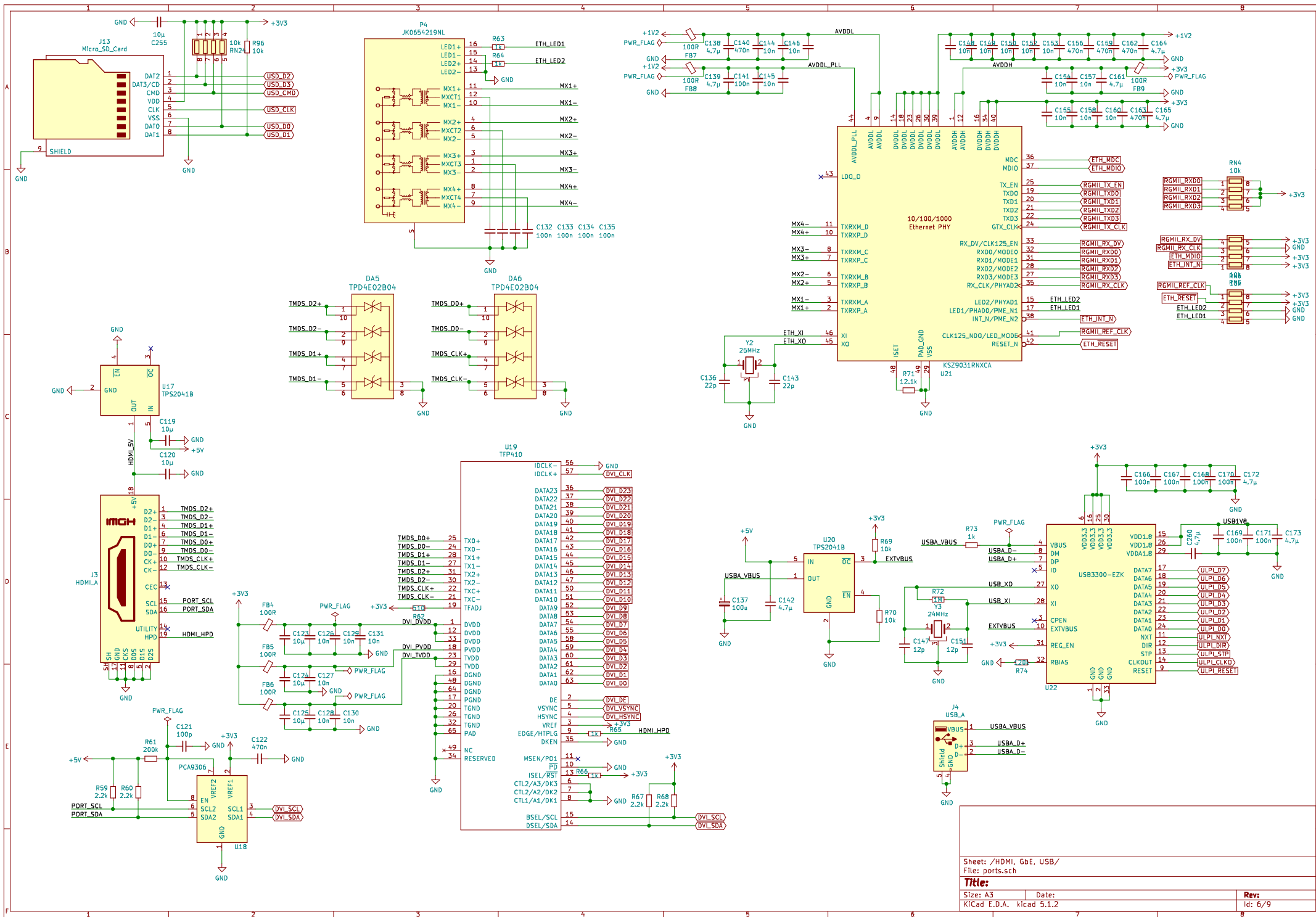
U15K
ECP5UM5G_85_CABGA756

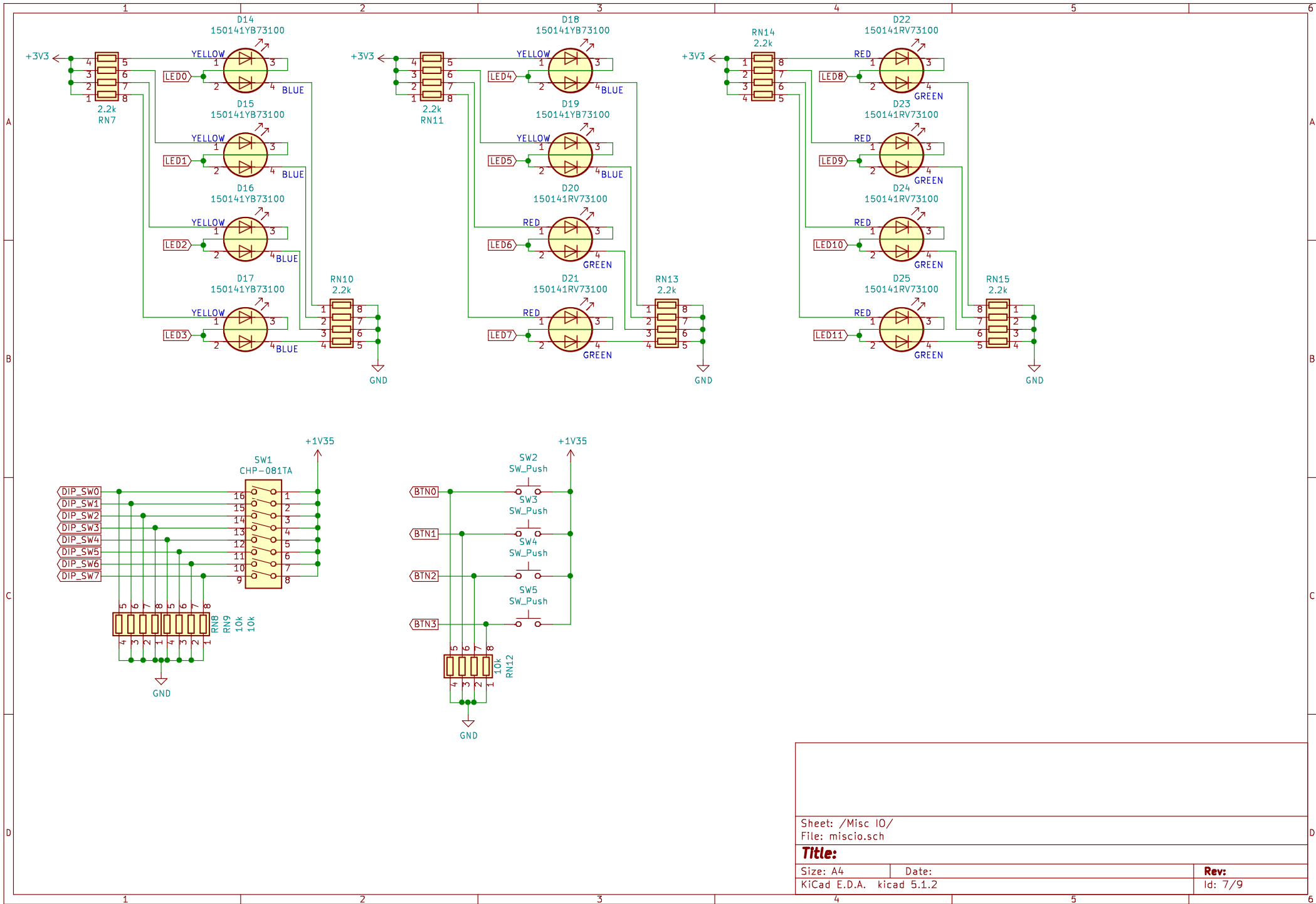


DCU1_TX0+	AK18	HDTXP0_D1CH0
DCU1_TX0-	AK19	HDTXN0_D1CH0
DCU1_RX0+	AM17	HDRXP0_D1CH0
DCU1_RX0-	AM18	HDRXN0_D1CH0
DCU1_TX1+	AM20	HDRXP0_D1CH1
DCU1_TX1-	AM21	HDTXN0_D1CH1
DCU1_RX1+	AK22	HDRXP0_D1CH1
DCU1_RX1-	AK23	HDTXN0_D1CH1
DCU1_REFCLK+	AM23	REFCLKP_D1
DCU1_REFCLK-	AM24	REFCLKN_D1

U15L
ECP5UM5G_85_CABGA756







Sheet: /Misc IO/
File: miscio.sch

Title:

Size: A4 Date:
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Rev:
Id: 7/9

